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CS33

Third Semester B.E. Degree Examination, June / July 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Show that EX-OR operation is not distributive over AND operation. **(04 Marks)**

b. State and explain the Shannon's Reduction theorem. **(04 Marks)**

c. Find the conjuctive and Disjunctive canonical forms of the expression: F(ABC) = AC + BC' **(06 Marks)**

d. Realize the EX – NOR function using only minimum number of i) Nand Gates ii) NOR Gates. **(06 Marks)**

2 a. Define i) Subsume ii) Prime implicant iii) Essential prime implicant. Give an example for each. **(06 Marks)**

b. Find the minimal conjunctive normal form for f(ABCD) = A ◯ B ◯ C ◯ D. Use K maps for specification. **(08 Marks)**

c. For the given Boolean function, determine a minimal sum using variable entered maps where x, y and z are map variables. **(06 Marks)**

$$f(ABxyz) = A\,\bar{x}\,\bar{y}\,\bar{z} + A\,\bar{x}\,\bar{y}\,z + A\,x\,\bar{y}\,z + \bar{B}\,\bar{x}\,\bar{y}\,z + B\,\bar{x}\,y\,\bar{z} + \bar{x}\,y\,z + x\,\bar{y}\,\bar{z}$$

3 a. Design a 4 input one output minimal gate combination network using only NAND GATES which has a 0 output when the majority of its inputs are at logic 1 and a 1 output when the majority of its inputs are logic 0. When the number of 1's and 0's are equal consider it as a don't care output. **(10 Marks)**

b. Design a stage of one Bit comparator which when cascaded helps in comparing two Binary numbers of any bit length. Draw the logic diagram. **(10 Marks)**

4 a. Design a full subtractor using 3 to 8 Decoder and Nand gates. **(10 Marks)**

b. Realize the two expression given $f_1(x\,y\,z) = \sum m(1, 2, 3, 7)$ and $f_2(x\,y\,z) = \sum m(0, 1, 2, 6)$. using PLA of the smallest size and draw the PLA table. **(10 Marks)**

5 a. What are the disadvantages of Totempole output? Draw and explain the logic diagram of a circuit, which removes the above disadvantage. **(10 Marks)**

b. Give a detailed comparison among LSTTL CMOS and ECL logic families highlighting the advantages of each for a given application. **(10 Marks)**

6 a. Draw a switch Debouncer using a SR latch and show the waveforms of switch Bounce and Debounce. **(10 Marks)**

b. Explain the advantages of an edge triggered flip flop over a pulse triggered flip-flop. **(04 Marks)**

c. Derive the characteristic equation of an SR flip flop and a JK flip flop. **(06 Marks)**

7 a. Design a Modulo – 6 self correcting counter whose counting sequence is 0 – 1 – 4 – 6 – 7 – 5 – 0. Use JK Flip Flops for realization. **(10 Marks)**

b. Draw the two forms of 3 bit shift register counters and explain their operation. **(10 Marks)**

8 a. Distinguish between Mealy and Moore model of clocked synchronous sequential network with block diagrams. **(08 Marks)**

b. State table shown refers to a clocked synchronous sequential network. Make a state assignment in binary code and find the excitation and output functions using JK flip flops. Draw the logic diagrams. **(12 Marks)**

PS	NS		Output	
	x = 0	x = 1	x = 0	x = 1
A	B	C	0	0
B	A	A	0	1
C	D	A	0	1
D	A	D	0	1

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